

REMARKS

Claims 1-42 are pending in the application. Claims 43-45 are newly added. Of the claims, Claims 1, 13, 25 and 38 are independent claims. Claim 38 has been rejected under 35 U.S.C. 101 because it does not describe a useful process, machine, manufacture or composition of matter. Claims 2-4, 6-11, 14-16, 26, 28-29, 31-36 and 39-42 have been objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 1, 5, 12-13, 17, 24-25, 27, 30 and 37-38 are rejected under 35 U.S.C. § 103(a) as being deemed unpatentable over Runaldue et al. (U.S. Patent Number 6,128,654.) That rejection is respectfully traversed and reconsideration is requested.

Regarding the rejection of claim 38 under 35 U.S.C. 101, claim 38 has been amended to recite "An apparatus for storing a pointer list." Removal of the rejection under 35 U.S.C. 101 and acceptance of Claim 38 as amended is respectfully requested.

The Applicant's disclosed queue includes a first memory having a first memory access time and a second memory having a second memory access time. Control logic enqueues in the queue a pointer to data to be transmitted by writing the pointer in the first memory, transfers the pointer to the second memory and dequeues the pointer from the second memory. (*See* Applicant's Specification Fig 4, 124, 300, 302.)

The cited prior art Runaldue is directed to a logical queue with three physical sections, a write side, a read side and an overflow area. The write side and read side are the on-chip portion of the logical queue and the overflow area is the off-chip portion of the logical queue. Pointers are added to the logical queue one at a time by writing to the write side and dequeued from the queue one at a time by reading from the read side. Pointers enqueued in the write side can be transferred directly from the read side to the write side or indirectly transferred through the overflow area. (*See* Fig. 4, output queue 74 write side 76, read side 72 and overflow area 110; and Col 8, line 28 – Col. 9, line 65.)

Runaldue's discussion of a logical queue does not teach or suggest the applicant's claimed "control logic which enqueues in the queue a pointer to data to be transmitted by writing the pointer in the first memory, transfers the pointer to the second memory and dequeues the

pointer from the second memory” as claimed by the Applicant in Claim 1. In the applicant’s claimed invention, pointers are enqueued in a first memory having a first access time and dequeued from a second memory having a second access time. In contrast, in the logical queue discussed by Runaldue, pointers are enqueued and dequeued from the on-chip portion of the logical queue, i.e. internal memory.

Claims 2-12 are dependent on Claim 1 and thus include this limitation over the prior art. Independent Claim 13 recites a like distinction in terms of a method and thus similarly patentably distinguishes over the prior art. Independent Claims 25 and 38 and Claims dependent on Claims 25 and 38 include like limitations distinguishing the cited art.

Applicant thanks the Examiner for the indication that claims 2-4, 6-11, 14-16, 26, 28-29, 31-36 and 39-42 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

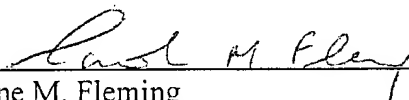
Accordingly, the present invention as now claimed is not believed to be anticipated by or made obvious from the cited art or any of the prior art. Removal of the rejections under 35 U.S.C. 103(a) and acceptance of Claims 1-45 is respectfully requested.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned.

Respectfully submitted,

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